REMARKS

Claims 34-38, 45-47 and 53 are pending in the present application.

Claim Rejections-35 U.S.C. 102

Claims 34-38 and 46 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Lin et al. reference (U.S. Patent No. 5,239,198). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 34 includes in combination a BGA (ball grid array) type semiconductor device; and a CSP (chip size packaged) type semiconductor device "mounted on an area of the backside surface of the base plate of said BGA type semiconductor device which does not have any bumps formed thereon, said CSP type semiconductor device having a semiconductor element which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals which are formed on the main surface, wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed". Applicants respectfully submit that the Lin et al. reference does not disclose these features.

The Examiner has relied upon Figs. 6 and 7 of the Lin et al. reference, and has alleged that the reference discloses a "CSP type semiconductor device having a semiconductor element 50" mounted on an area of the backside of the base plate of the BGA type semiconductor device. However, as emphasized in the Remarks section beginning on page 7 of the Amendment dated March 24, 2005, and as described

beginning in column 6, line 61 of the Lin et al. reference, **element 50 is a passive electronic component, such as a resistor, a diode, a decoupling capacitor, or the like**. The Lin et al. reference does not describe passive electronic component 50 as a semiconductor device. Applicants respectfully submit that passive electronic component 50 of the Lin et al. reference is not a CSP (chip size packaged) type semiconductor device having a semiconductor element, as would be understood by one of ordinary skill.

Particularly, enclosed is an excerpt from the Wolf et al. text "Silicon Processing For The VLSI Era, Volume 1: Process Technology". Fig. 17-27 of the Wolf et al. text illustrates a chip-scale (size) package (CSP) as would be understood by one or ordinary skill. As shown, the CSP package includes a die formed on a first side of the substrate, with solder balls formed on the other side of the substrate, whereby bond wire, the die and the first side of the substrate are sealed with a molding compound.

Clearly, passive electronic component 50 of the Lin et al. reference is not a CSP package as would be understood by one of ordinary skill, because passive electronic component 50 does not include the above noted features of art recognized CSP packages as exemplified by the Wolf et al. text. The Lin et al. reference as relied upon by the Examiner thus does not provide high density packaging using different types of semiconductor devices such as BGA and CSP types. The Lin et al. reference does not provide a high performance device utilizing the functions of both BGA and CSP type devices in a single, small high density package, as in claim 34. Applicants therefore

respectfully submit that the semiconductor device of claim 34 distinguishes over the Lin et al. reference, and that this rejection of claims 34-38 and 46 is improper for at least these reasons.

In the current Office Action dated April 19, 2005, the Examiner has merely repeated the above noted rejection word for word from the previous Office Action dated November 24, 2004, without acknowledging or addressing the traversal as presented in the Amendment dated March 24, 2005. It would thus appear that the Examiner has completely disregarded the arguments presented in the Amendment dated March 24, 2005. This rejection has thus been repeated without acknowledgment of the presented arguments and without the substance of the arguments addressed by the Examiner, contrary to the guidelines as set forth in Manual of Patent Examining Procedure section 707.07(f). **If this rejection is to be maintained, the Examiner is respectfully requested to establish on the record how passive electronic component 50 of the Lin et al. reference may be interpreted as a CSP package**.

Claim Rejections-35 U.S.C. 103

Claims 45-47 and 53 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Lin et al. reference in view of the Schrock reference (U.S. Patent No. 5,861,678). This rejection is respectfully traversed for the following reasons.

The Examiner has relied upon Figs. 4A and 4B of the Schrock reference. However, as described beginning in column 3, line 64 through to column 4, line 3 of the

Schrock reference, the device as illustrated in Figs. 3A – 4B includes die 10 having substrate 30 mounted thereon. Substrate 30 comprises an electrically insulating material such as ceramic, and can be provided in the configuration of a printed circuit board (PCB), or in the configuration of a multi-chip-module (MCM).

As emphasized in the Amendment dated March 24, 2005, Figs. 4A and 4B of the Schrock reference as relied upon by the Examiner are not specifically described as including a BGA (ball grid array) type semiconductor device having a CSP (chip size package) type semiconductor device mounted thereon, in an area which does not have any bumps formed thereon. Particularly, substrate 30 of the Schrock reference is not specifically described as a BGA (ball grid array) type semiconductor device including a semiconductor die on a base plate and a plurality of bumps formed on a backside surface of the base plate, as would be necessary to meet the features of claim 34. The Schrock reference thus does not include a BGA semiconductor device as would be understood by one of ordinary skill.

Moreover, die 10 of the Schrock reference is not a CSP device as would be understood by one of ordinary skill. The Schrock reference would thus provide no motivation to modify the Lin et al. reference to provide a high performance device utilizing the functions of both BGA and CSP type devices in a single, small high density package. Applicants therefore respectfully submit that the semiconductor device of claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 45-47 and 53 is

improper for at least these reasons, in addition to the reasons previously set forth above. **If this rejection is to be maintained, the Examiner is respectfully requested to clearly establish on the record how the Schrock reference may be interpreted as including both BGA and CSP packages**.

Claim 53, as dependent upon claim 34, features "the main surface of the semiconductor element is sealed with a resin, and portions of each of the plurality of terminals are exposed from the resin". Applicants respectfully submit that bonded connections 44 of die 10 in Fig. 4B of the Schrock reference do not have portions thereof exposed from adhesive layer 40. That is, bonded connections 44 are completely enveloped within adhesive layer 40. Contrary to the Examiner's apparent assertion by way of the illustration at the bottom of page 4 of the Office Action dated April 19, 2005, terminals 44 of die 10 in Fig. 4B of the Schrock reference do not have portions exposed from adhesive layer 40. Applicants therefore respectfully submit that claim 53 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner, for at least these additional reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present

application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.126(a), the Applicants hereby petition for an extension of one (1) month to August 19, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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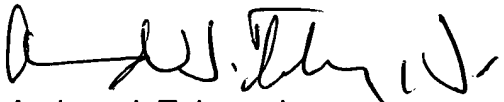

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Enclosures: Excerpt from the Wolf et al. text